Abstract of the Disclosure

Provided are a dual damascene interconnection with a metal-insulator-metal (MIM) capacitor and a method of fabricating the same. In this structure, an MIM capacitor is formed on a via-level IMD. After the via-level IMD is formed, while an alignment key used for patterning the MIM capacitor is being formed, a via hole is formed to connect a lower electrode of the MIM capacitor and an interconnection disposed under the via-level IMD. Also, an upper electrode of the MIM capacitor is directly connected to an upper metal interconnection during a dual damascene process.

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